

PLANAR MMIC HYBRID CIRCUIT AND FREQUENCY CONVERTER

Tetsuo Hirota Hiroyo Ogawa
Yoshiaki Tarusawa Kuniki Owada

NTT Electrical Communication Laboratories
Nippon Telegraph and Telephone Corporation
Yokosuka, Japan

ABSTRACT

A "planar" circuit configuration for MMIC (Monolithic Microwave Integrated Circuit) has been proposed. It uses coplanar waveguides and slotlines on the upper side of the substrate. Novel hybrid circuits have been fabricated. It has also been shown that small sized, balanced FET circuits can be achieved.

INTRODUCTION

The development of high-performance and low-cost microwave circuits have been required for new radio communication systems. Monolithic Microwave Integrated Circuits (MMIC's) offer the potential to meet this demand.

In this paper, a "planar" circuit configuration for MMIC is proposed. It employs coplanar waveguides and slotlines on the upper side of the substrate, and has the same functions as those of double-sided MIC's (1),(2). The merits of this configuration are induced from a combination of balanced lines (slotline, etc.) and unbalanced lines (coplanar waveguide, etc.).

This paper describes how balanced frequency multiplier, balanced up-converter as well as hybrid circuits can be developed in compact size using the aforementioned "planar MMIC" configuration.

PLANAR MMIC

A coplanar waveguide and a slotline have the advantage of easy grounding without via-holes. This is an important practical merit in MMIC, where many source-grounded FET's and shorted stubs are used. Moreover, on-wafer testing and screening are, consequently, possible. On the other hand, straps to interconnect conductors of different transmission lines

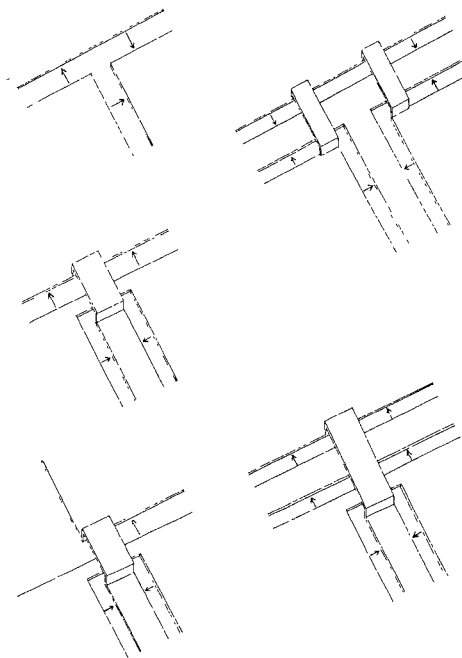


Figure 1. Transmission-line junctions usable in planar MMIC's.

or two ground planes are frequently required. This is the main reason why the coplanar waveguide has been less popular than the microstrip line. Such a strap, however, can precisely be formed in MMIC using air-bridge technique.

Application of slotlines to MMIC in addition to coplanar waveguides makes it possible to obtain series T junctions as well as signals in anti-phase. This is of great merit for the design of magic T and balanced circuits. Figure 1 shows the basic transmission-line junctions usable in planar MMIC's.

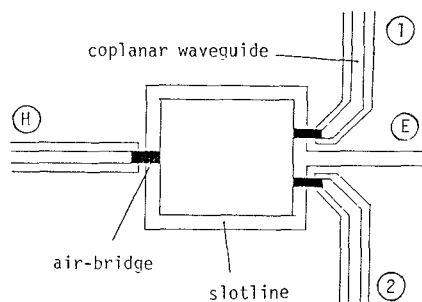


Figure 2. Layout of a planar magic T.

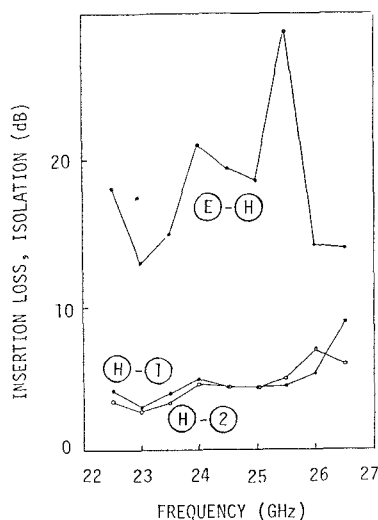


Figure 3. Measured performance of the magic T.

MAGIC T AND BRANCH-LINE COUPLER

Figure 2 shows the layout of a planar magic T. The measured performance of the 26 GHz band magic T is shown in Figure 3, having employed a slotline T junction for the E-port, with air-bridges used to interconnect slotlines and coplanar waveguides.

The 26 GHz band branch-line hybrid coupler and its performance are shown in Figures 4 and 5. This coupler consists of coplanar waveguide input/output ports and quarter-wavelength slotlines.

BALANCED FET CIRCUITS

A balanced FET frequency multiplier and a balanced FET up-converter are designed and fabricated using planar MMIC technique. Balanced configuration is suitable for the MMIC because (1)

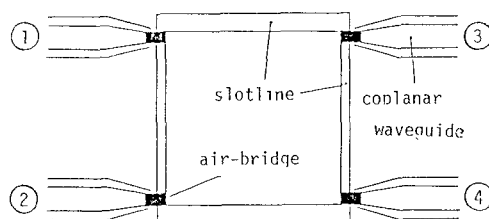


Figure 4. Layout of a branch-line hybrid coupler.

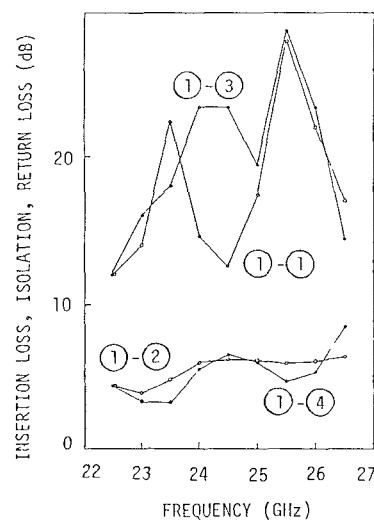


Figure 5. Measured performance of the hybrid coupler.

circuit cost is not strong dependent upon the number of FET's, (2) LO frequency signal can be suppressed without filters (MMIC filters with good performance are not obtainable). If a balanced circuit is designed conventionally using microstrip lines, a large balun circuit or hybrid circuit is necessary. Since circuit size is a great factor affecting IC cost, it represents a major obstacle regarding development of a low-cost MMIC up-converter.

The planar configuration presents a way to overcome this problem. Figure 6 is an example of a planar balanced frequency multiplier chip, using a slotline in the input port. 13 GHz input signals in anti-phase are fed to the two FET's through the slotline and a lumped-constant matching circuit consisting of spiral inductors and MIM (metal-insulator-metal) capacitors. The 26 GHz output signal is obtained from a coplanar waveguide. The measured performance of the frequency multiplier is shown in Figure 7. Circuit size is about 1.0 mm \times 1.5 mm.

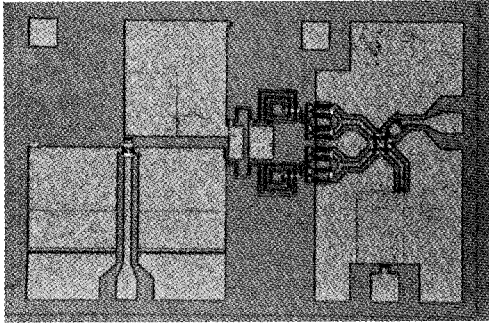


Figure 6. Balanced FET frequency multiplier chip.

Another example of a planar MMIC is a balanced FET frequency up-converter. The circuit is shown in Figure 8. As in the frequency multiplier, it uses a slotline in the input circuit. LO signals in anti-phase can easily be obtained from a simple slotline T junction. In the output circuit, up-converted signals are combined in phase by a coplanar waveguide T junction. Stubs are short-circuited by MIM capacitors. DC power and IF signals are supplied through this stubs. Circuit size is about 1.3 mm \times 1.8 mm at the LO frequency of 26 GHz.

CONCLUSION

A planar circuit configuration for MMIC has been proposed. It uses coplanar waveguides and slotlines on the upper side of the substrate, combined by precisely fabricated air-bridges. Novel hybrid circuits for this planar configuration have been fabricated and tested. It has been shown that a small sized, balanced FET frequency multiplier and up-

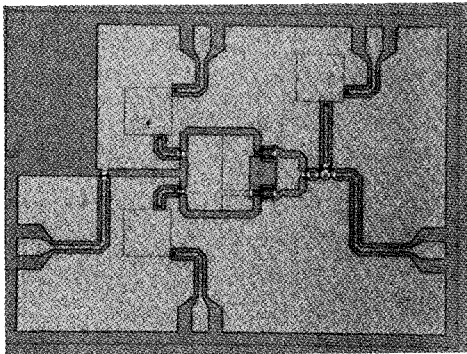


Figure 8. Balanced FET up-converter chip.

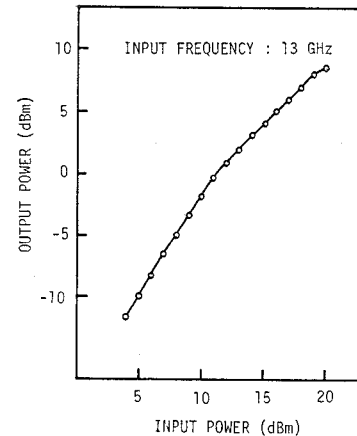
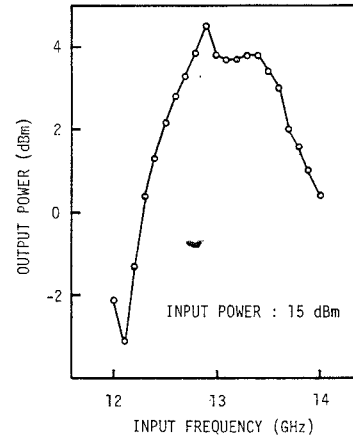


Figure 7. Measured performance of the frequency multiplier.

converter can be achieved using coplanar waveguides and slotlines. These planar MMIC's need no via-holes for grounding and can be tested via on-wafer method.

ACKNOWLEDGEMENT

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